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The annealing effect on properties of ZnO thin film transistors with Ti/Pt source-drain contact

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Abstract ZnO-based thin film transistors (TFTs) with Ti/Pt contacts were fabricated on SiO_2/Si substrates. The as-deposited ZnO TFT did not work well as a TFT device but the annealed ZnO TFT showed acceptable characteristics with a mobility (μ_{sat}), threshold voltage (V_{th}), on/off ratio and subthreshold swing (SS) of 0.8 cm^2/V.s, 2.5 V, over 10^6 and 0.84 V/dec, respectively. Complete oxygen loss was observed in ZnO after annealing at 300°C under a N_2 atmosphere. The annealing process altered the crystallinity, density and composition of the ZnO active layers due to the formation of oxygen vacancies as shallow donors. This process is expected to play an important role in controlling the TFT performance of ZnO. In addition, it is expected to form the basis of the future electronic devices applications, such as transparent displays and active matrix organic lighting emitted displays (AMOLED).

Keywords Thin film transistor · ZnO · Ti contact · Annealing

1 Introduction

ZnO has attracted considerable interested for a range of applications, such as UV light emitters, spintronic devices, transparent high-power electronics, surface acoustic wave devices, piezoelectronic transducers, gas and biological sensors, solar cells and thin film transistor devices [1–7]. ZnO based thin film transistors (TFTs) are particularly attractive because good quality polycrystalline films [8] with moderate Hall mobility (>1 cm^2/V.s) can be made at room temperature, and there is good compatibility with plastic or flexible substrate materials. In addition, there has been interest in transparent TFTs because the ZnO semiconductor is transparent in the visible range and is less light sensitive [9].

ZnO thin films as a TFT channel layer has several advantages over amorphous silicon films. For example, ZnO-based TFTs may exceed conventional amorphous Si TFTs in terms of the field-effect mobility, leading to higher drive currents and faster device operating speeds. The deposition process can also be carried out at room temperature, which may decrease the TFT fabrication cost by replacing with conventional glass [9]. In addition, it is possible to realize new display devices, such as flexible and transparent electronic devices.

Until now, most ZnO channel layers in TFTs have been deposited by substrate heating or subjected to post-thermal annealing, mainly to increase the crystallinity and mobility of the ZnO layer. However, a few groups reported a relationship between the performance of ZnO-based TFTs and the annealing process [10–12], even though the thermal process is one of the most important factors for intrinsically controlling the ZnO channel layer. In this study, well-performed ZnO TFTs were fabricated by post-annealing at 300°C in a N_2 atmosphere. The post-annealing process improves the electrical performance of ZnO TFTs induced from the physical change in the ZnO channel layer itself.

2 Experiment

The ZnO-based TFTs as a gate electrode were fabricated on 4" n+ doped silicon wafer. A 100 nm thick SiO_2 layer as a gate insulator layer was grown conventionally on a silicon wafer by thermal CVD. A ZnO active layer (70 nm) was

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deposited on the SiO_2/Si wafer by RF sputtering at a power of 200 W, working pressure of 5 mTorr, and an O_2/Ar (ratio= 0.012) atmosphere at room temperature. The ZnO active and source/drain (S/D) regions were defined using photolithography and lift-off processes, respectively. The S/D electrodes with electron-beam evaporated Ti (10 nm) / Pt (100 nm) were formed using a lift-off process. Figure 1(a) shows a schematic diagram of the ZnO TFT structure with a bottom gate and top contact. Figure 1(b) shows a top-view micrograph of a TFT with a channel length (L) and width (W)of 20 μm and 50 μm, respectively. The transfer curves (V_{GS} (gate voltage) vs I_{DS} (drain current)) of the ZnO TFTs were measured using a Keithley 4200 parameter analyzer system before and after annealing the ZnO TFTs. The fabricated ZnO TFTs were annealed at 300°C for 1 h under a N_2 atmosphere to have good electrical performance. The crystalline structures and size of the ZnO thin films were examined by x-ray diffraction (XRD). The density and roughness on each ZnO film was measured and extracted by x-ray reflectivity (XRR). The cross-sectional microstructure of the interface between each layer was analyzed by transmission electron microscopy (TEM). The depth-profiles of the cross-sectional ZnO layers were analyzed by auger electron spectroscopy (AES) and energy dispersive x-ray spectroscopy (TEM-EDX).

3 Results and discussion

Figure 2 shows the transfer (V_{GS} vs I_{DS}) and output (V_{DS} vs I_{DS}) curves of the ZnO TFTs before and after the 300°C post-annealing process. All TFT devices were measured with a channel length and width of 4 μm and 50 μm, respectively. As the gate voltage varies widely from −30 V to 50 V in Fig. 2(a), the as-deposited ZnO TFTs did not show any drain current under an applied drain voltage, which is similar to an insulator layer (below 10^{-12} A). The ZnO films deposited under these deposition conditions, showed very high resistivity (over 10^8 Ω cm), making it impossible to measure the hall mobility (this value being out of range of the Hall-effect equipment used). The ZnO TFTs were then heated to 300°C for 1 h in a N_2 atmosphere. As shown in Fig. 2(b), the ZnO films exhibited good TFT operations with on-to-off current ratios >10^6 and a low sub-threshold gate voltage swing (SS) of 0.84 V/decade. The mobility and threshold voltage were extracted using the follow equation and by fitting a straight line to a plot of the square root of I_{DS} vs. V_{GS}, respectively.

$$I_{DS} = C_{OX} \frac{W}{2L} \mu_{SAT} (V_G - V_{TH})^2, \quad V_{DS} > V_{GS} - V_{TH} \qquad (1)$$

where C_{ox} is the gate insulator capacitance per unit area [F/cm^2].

A threshold voltage (V_{th}) and mobility (μ_{SAT}) in the saturation region (V_{DS} > V_{GS}−V_{th}) were calculated to be 2.5 V and 0.8 cm^2/V.sec, respectively, showing n-type enhancement mode and a hard saturation current at the post pinch-off voltage. Figure 2(c) shows the I_{DS} curves as a function of the drain voltage (V_{DS}) for different V_{GS} values. The saturation behavior was obtained under a gate bias of 20 V. The device exhibited full saturation, as evidenced by the flatness of the slope of each I_{DS} curve at a large V_{DS}. Surprisingly, the N_2 annealing process caused significant changes in the ZnO TFT performance. It is possible to consider some of the changes in the ZnO channel and contact layer because as-deposited TFT did not show any drain current flow.

To understand the change in the ZnO TFTs, both 80 nm thick ZnO active layers on silicon substrates (i.e. as-deposited and annealed at 300°C) were analyzed by XRD and XRR. As shown in Fig. 3, all thin films showed two peaks, which were assigned to the ZnO (002) and (103) orientations. The diameter of the ZnO grains increased from 103 (as-deposited) to 124 Å (annealed), as calculated from λ/(FWHM (full width at half maximum)×cosθ). After annealing at 300°C, the position of both peaks shifted to a larger angle (for example, 2θ=33.86° [as-deposited] to 34.20° [annealed] in ZnO (0002) plane). This shift means that the lattice constant *a* and *c* decreases after annealing. In addition, the band gap energies (E_g) of the ZnO films were calculated by fitting the sharp adsorption edges (not shown here). The E_g of the ZnO films also decreased from 3.13 eV to 3.04 eV after annealing. This phenomenon might be due to the increased crystallinity of the ZnO films because the

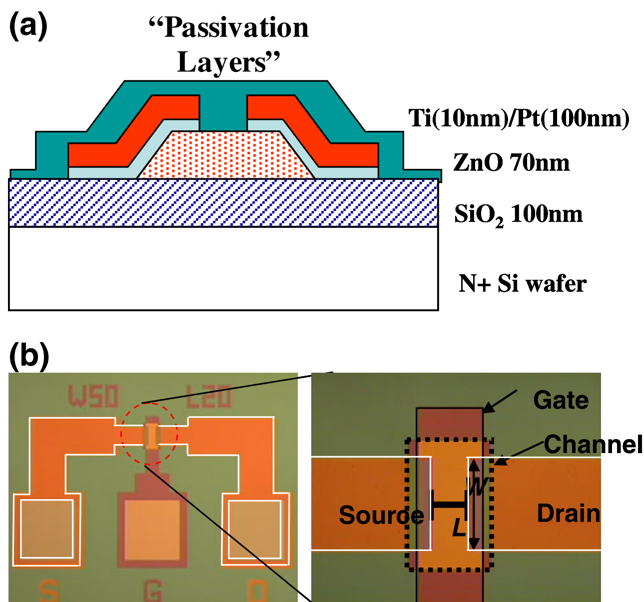

Fig. 1 (**a**) The cross-sectional diagram of ZnO thin film transistors (TFTs) (**b**) Planar microscopy of ZnO TFTs

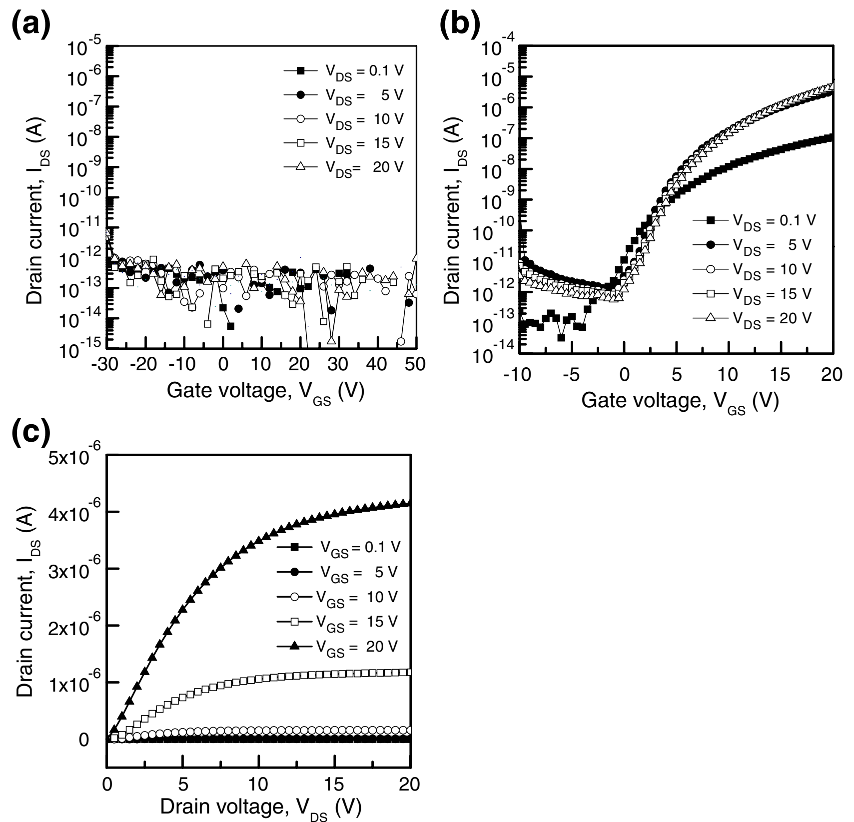

Fig. 2 (**a**) The transfer curve (V_{GS} vs I_{DS}) on the as-deposited ZnO thin film transistors (TFTs). (**b**) The transfer curve after annealing at 300°C under N_2 atmosphere. (**c**) The output curve (V_{DS} vd I_{DS}) on annealed ZnO TFTs

band gap decreases with decreasing lattice constant. These results are consistent with other reports [13, 14].

However, XRR showed that the density of the annealed films was quite different; the density of the as-deposited and annealed ZnO films was 5.456 g/cm^3 and 5.37 g/cm^3, respectively. The density of thin films generally increases after thermal annealing or increasing film crystallinity.

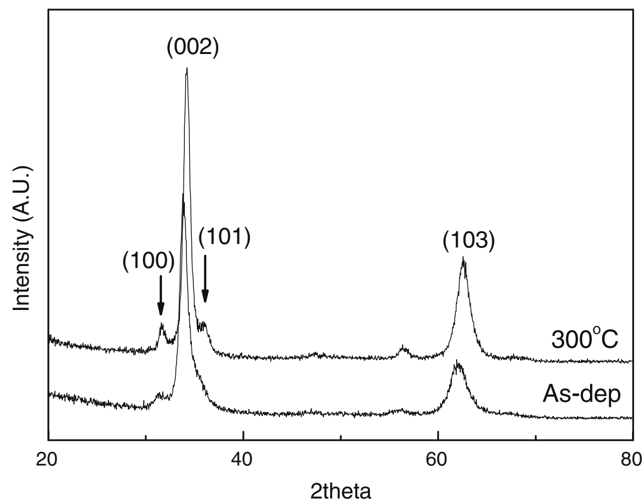

Fig. 3 X-ray diffraction patterns (XRD) of the ZnO thin films before and after 300°C annealing

However, the density can increase if some atoms in the films become loose and decrease as a result of a reaction or thermal activation. ZnO is a well-known n-type semiconductor due to native defects, such as oxygen vacancies (V_O) and Zn interstitials (Zn_i). Therefore, it is believed that a N_2 annealing process can help create more native defects (oxygen vacancies rather than Zn interstitials) in the ZnO films due to the decreasing film density. This concurs with the AES results, which showed that the O/Zn ratio in annealed ZnO films was approximately 95% of the as-deposited ratio (data not shown). The other result also suggests that annealing above 300°C can create considerable mass loss from ZnO due to oxygen evaporation [15]. This means that the annealing process would affect the ZnO active layer of TFTs directly to increase the electron carrier concentration due to the increasing number of oxygen vacancies.

Figure 4(a)–(d) show cross-sectional TEM images and the lateral profile of the ZnO composition before and after annealing. As shown in Fig. 4(c), relative oxygen loss on the ZnO contact area was observed only in the as-deposited state due to the formation of thin titanium oxide layer. A smooth as-deposited interface between the ZnO and Ti layers has no intermixed zone but oxygen loss can occur at the interface. Thin titanium oxide layers may be formed at the metal/ZnO interface because titanium has a higher

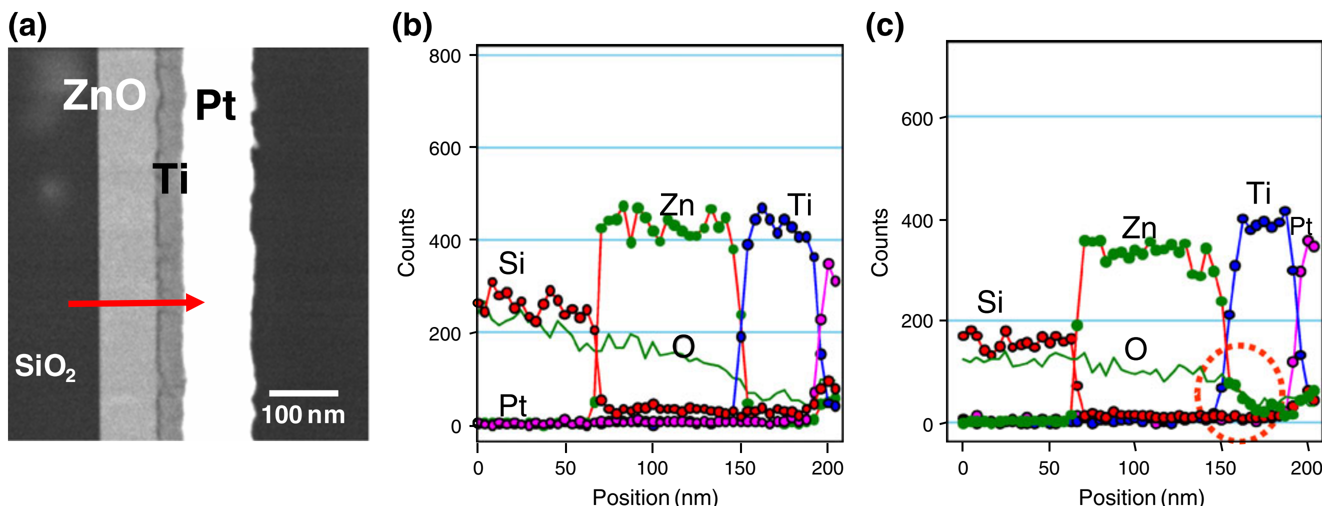

Fig. 4 The cross-sectional transmittance electron microscopy (TEM) of (**a**) as-deposited ZnO thin film transistor (TFT) and (**b**) annealed ZnO TFT. The lateral composition profile of ZnO layers at (**c**) as-deposited TFT and (**d**) annealed TFT. (The *arrow* means the direction of the depth profile while analyzing the ZnO samples)

affinity to oxygen than Zn [16]. However, in Fig. 4(d), oxygen loss occurred only in the ZnO active layers after annealing under a N_2 atmosphere. Many oxygen vacancies can exist in the ZnO active layer. Annealing would accelerate the increase in shallow donors, such as oxygen vacancies and Zn interstitials [17–19]. This suggests that the as-deposited ZnO active layer has a low carrier concentration similar to an insulator, which is insufficient to work as a channel layer.

Figure 5(a) shows the cross-sectional TEM image around the as-deposited TFT contact areas. Sharp and smooth interfaces between the ZnO and Ti/Pt were observed. As shown in Fig. 5(b) and (c), TEM-EDX shows the depth profile of the composition at the contact

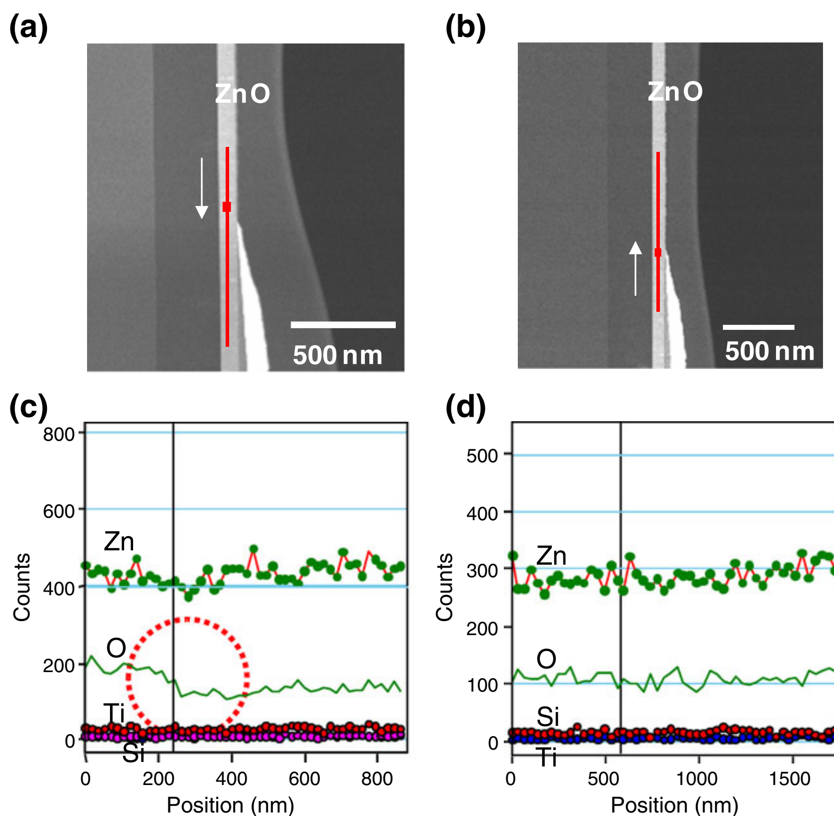

Fig. 5 (**a**) Cross-sectional transmittance electron microscopy (TEM) of an as-deposited ZnO thin film transistor (TFT) in Pt/Ti/ZnO/SiO_2 (contact area) (**b**) The depth-profile of cross-sectional ZnO TFTs contact area before annealing (**c**) Depth-profile of cross-sectional ZnO TFTs contact area after annealing (The *red-line* in figures is the area of depth-profiling and the *arrow* means the direction of depth-profile)

areas before and after annealing. An intermixed interface layer was also observed after annealing. Oxygen is removed predominantly from the ZnO surface and Zn atoms migrate into the Ti layer. The thin titanium oxide interface layers and out-diffusion of Zn may result in oxygen vacancies near ZnO, which are effective electron donors. This would reduce the specific contact resistivity that plays an important role in improving the TFT performance. Therefore, annealing at 300°C would help create oxygen vacancies (V_O) to produce ohmic Ti/Pt contact [20]. In addition, annealing has altered the composition ratio of the ZnO active layer to be a Zn rich phase. Therefore, a N_2 annealing process under 300°C can improve the performance of ZnO TFTs by increasing the carrier concentration and forming ohmic contact in ZnO films.

4 Conclusion

In summary, good quality ZnO TFTs were developed after annealing, and the influence of annealing on the ZnO TFTs was investigated. The annealing process altered the crystallinity, density and composition of the ZnO active layers. This results from the formation of oxygen vacancies as a shallow donor and will play an important role in controlling the performance of ZnO TFTs. These results will help fabricate and optimize high performance ZnO TFTs. Moreover, it is expected to form the basis for the future electronic devices applications, such as transparent displays and active matrix organic lighting emitted displays (AMOLED).

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